Examiner Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Michael Byorick on 1/15/09.

Amendment to the following claims:

As per claim 1:

1. A method for detecting computational errors in a system comprising a digital processor executing a program, the method comprising steps of:

separating the program in computation segments;

compiling source code for at least one of the segments to generate two code sections, one of which is functionally redundant with respect to the other; and

generating comparison code for comparing results produced by execution of the two code sections;

wherein the processor is configured to: ~~executing~~ execute each of the code sections in a different computational domain to generate respective results; ~~comparing~~ compare the respective results using the comparison code to detect said computational errors; and ~~executing~~ execute one of the code sections to alter further flow of execution of the program only if the respective results are identical.

As per claim 18:

18. A system for detecting computational errors in a digital processor executing a program, the system comprising a compiler executing on a processor configured to:

separate the program into computation segments;

compile source code for at least one of the computation segments to generate output comprising two redundant code sections, each of which is configured to execute in a different computational domain; and generate comparison code for

comparing respective results produced by execution of the two code sections; ~~and~~

indicate that one of said computational errors has been detected when the respective results are different.

As per claim 31:

31. A system for detecting computational errors in a digital processor executing a program, the system comprising;

means for compiling source code for at least part of the program to generate two code sections, one of which is functionally redundant with respect to the other;

means for generating comparison code for comparing results produced by execution of the two code sections; wherein each of the code sections is executed by the processor in a different computational domain to generate respective results;

means for comparing the respective results using the comparison code to detect said computational errors; and

means for performing error handling, if a discrepancy between the respective results is found.

As per claim 34:

34. Computer product code ~~A software product~~ in a system comprising instructions, stored on a computer-readable storage media, wherein the instructions, when executed by a ~~computer~~ digital processor, perform steps for detecting computational errors in a the digital processor executing a program, comprising:

compiling source code for at least part of the program to generate two code sections, one of which is functionally redundant with respect to the other;

generating comparison code for comparing results produced by execution of the two code sections;

wherein the processor is configured to: ~~executing~~ execute each of the code sections in a different computational domain to generate respective results; ~~comparing~~ compare the respective results using the comparison code to detect said computational errors; an ~~performing~~ perform error handling, if a discrepancy between the respective results is found.

Response to Arguments

1. Applicant's argument filed on 10/22/08 has been fully considered and they are found persuasive.

Reasons for allowance

2. Claims **1-36** are allowable over the prior art. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art is exemplified by Bunnel et al. (U.S. Patent No. 5,594,903) and Galpin (U.S. Patent No. 7,043,728).

As per claim 1:

Bunnel et al. teaches within a memory portion an executable image of the operating system. The operating system is next to an interrupt vector table, wherein dynamic execution support of the operating system is provided by virtual memory page address translation tables. Further, an operating system boot loader is positioned within the memory at a default address. The boot leader loads the operating system from a storage medium, wherein the storage medium is ROM. Further, the boot loader program transfers execution of control over the (CPU) to a predefined operating system execution entry point.

Galpin teaches executing a first sequence of instructions in a fixed process or thread and executing a second sequence of instructions in a second process. The processes can operate in different processors. Further, the states of the first and second processors are compared. The states can include registers, memory and flags just to name a few, in order to see if the two processes executed their respective sequences substantially identically, and are ready to begin execution of additional sequences.

However, the two references mentioned above whether alone or in combination do not teach *"compiling source code for at least one of the segments to generate two code sections, one of which is functionally redundant with respect to the other; execute each of the code sections in a different computational domain to generate respective results; compare the respective results using the comparison code to detect said computational errors; and execute one of the code*

sections to alter further flow of execution of the program only if the respective results are identical.

Dependent claims **2-17** depend from allowable independent claim and inherently include limitations therein and therefore are allowed as well.

Independent claims **18, 31 and 34** are also allowable for having similar limitations to claim

Dependent claims 19-30, 32-33 and 35-36 depend from allowable independent claim and inherently include limitations therein and therefore are allowed as well.

Conclusion

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Enam Ahmed whose telephone number is 571-270-1729. The examiner can normally be reached on Mon-Fri from 8:30 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques, can be reached on 571-272-6962.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

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EA

1/21/09

/Esaw T Abraham/

Primary Examiner, Art Unit 2112